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FINAL REPORT

TIROS OPERATIONAL VERTICAL SOUNDER
SUBTASK: Instrument Sequencing and
Control Study

GULTON INDUSTRIES INC.

DATA SYSTEMS DIVISION 15000 CENTRAL EAST, ALBUQUERQUE, N. M. 87112

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TIROS OPERATIONAL VERTICAL SOUNDER
SUBTASK: Instrument Sequencing and
Control Study

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FOREWORD

This report is the result of a logic design study for the TIROS-N Operational Vertical Sounder. The study was conducted by Gulton Industries, Data Systems Division, under contract to the National Oceanic and Atmospheric Agency, National Environmental Satellite Service. This study is one part of the effort directed at total electronic design of the instrument.

The design to the functional level allows the specification of data and control interfaces as well as power requirements. Implementation of the required functions does not push the state of the art in any sense; good design practice should result in a control system with the utmost in reliability.

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SYSTEM TIMING AND CONTROL REQUIREMENTS

Control of the instrument subsystems is performed by a centralized, synchronous, logic network, denoted as the System Timing and Control Unit.

General: Control and timing logic is required to keep all aspects of the TOVS signal processing in proper synchronism with the TIROS-N Information Processor (TIP), and TOVS scan program, and the optical chopper. The TOVS requires two (2) externally supplied control signals:

- TIP - Master Frame Sync (16 second period)
- S/C Clock - 1248 KHZ signal

Using these signals as a basis, the TOVS system timing and control unit will develop all the necessary instrument control signals. The main control signals and their functions are identified as follows:

a) Integrate, Dump and Hold: Controls the analog data integrators.
b) Advance Multiplexer: Controls the analog multiplexer.
c) Start Conversion: Used to initiate the ADC conversion.
d) Scan Step Rate: Advances the scan mirror.
e) Chopper Rate: Advances the chopper motor.

Description: A block diagram illustrating the Timing and Control unit configuration is shown in Figure A on the adjacent page. Note that three (3) basic functions are performed;

(1) Wave shapers are used to buffer the externally supplied clock (1248KHZ) and master frame sync pulse (MFSP).
(2) A counting register comprised of several stages generates all the necessary frequencies from 1248KHZ to 1/264 HZ.
(3) Logic gates are used to develop the desired control signals by decoding the various counter chain states.

The exact logic structure of the counter stages and associated decoding gates can be synthesized several ways. Care must be exercised to avoid false signals from the decoding gate, due to logic element propagation delays.

Note that the system timing signals have a fixed known relationship relative to each other and are synchronized to the MFSP signal.

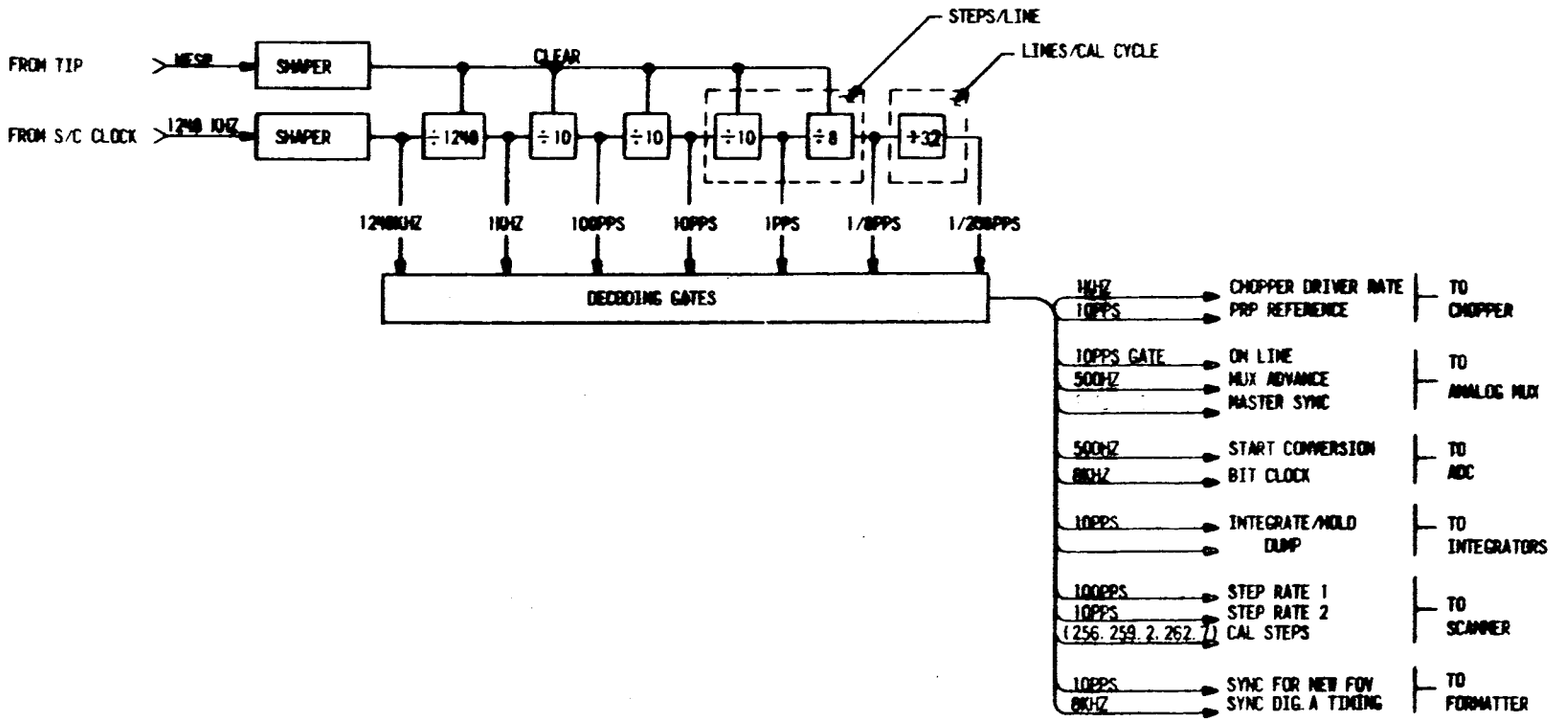


FIGURE A
SYSTEM TIMING
AND CONTROL

Section 1- Instrument Sequencing and Control

DESCRIPTION OF SYSTEM TIMING

A timing diagram is presented to clarify the fundamental instrument control timing requirements.

General: A timing diagram illustrating the phase relation of the key control signals is shown in Figure A. The scan mirror step rate, PRP chopper signal, integrator controls, and data processing signals are identified. Scan steps occur every 100 ms. This interval is subdivided into three (3) segments; 1) 75 ms used for data integration, 2) 18.75 ms used to digitize the 16 data channels and 3) 6.25 ms allocated for dumping the integrators.

Scan Mirror Step: This signal occurs at a 10 pps rate during the normal scan cycle and at a 100 pps rate during the retrace cycle.

PRP Signal: This signal is derived directly from the chopper mechanism and is controlled to maintain phase sync with the integrator control signal. Signal occurs at a 40 Hz rate.

Integrator Controls: Infrared energy integrators perform the integration function for 75 ms, hold the integrated value for a period of 18.75 ms, and are reset to zero during the next 6.25 ms period. A time delay of 31.25 ms is inserted between the scan step signal and the integration period. This dalay allows to scan mechanism to settle to a static value before data processing occurs.

Multiplexer Controls: Analog data will be processed during the 18.75 ms HOLD period. Three signals control the analog multiplexers, i.e., 10 pps ON LINE signal, 500 Hz multiplexer advance signal, and the 1/256 Hz master sync signal.

ADC Controls: The ADC and multiplexer operate in conjunction to digitize the analog data. A start conversion signal (500 Hz, gated) is developed for each sample; plus an 8 kHz bit trial clock.

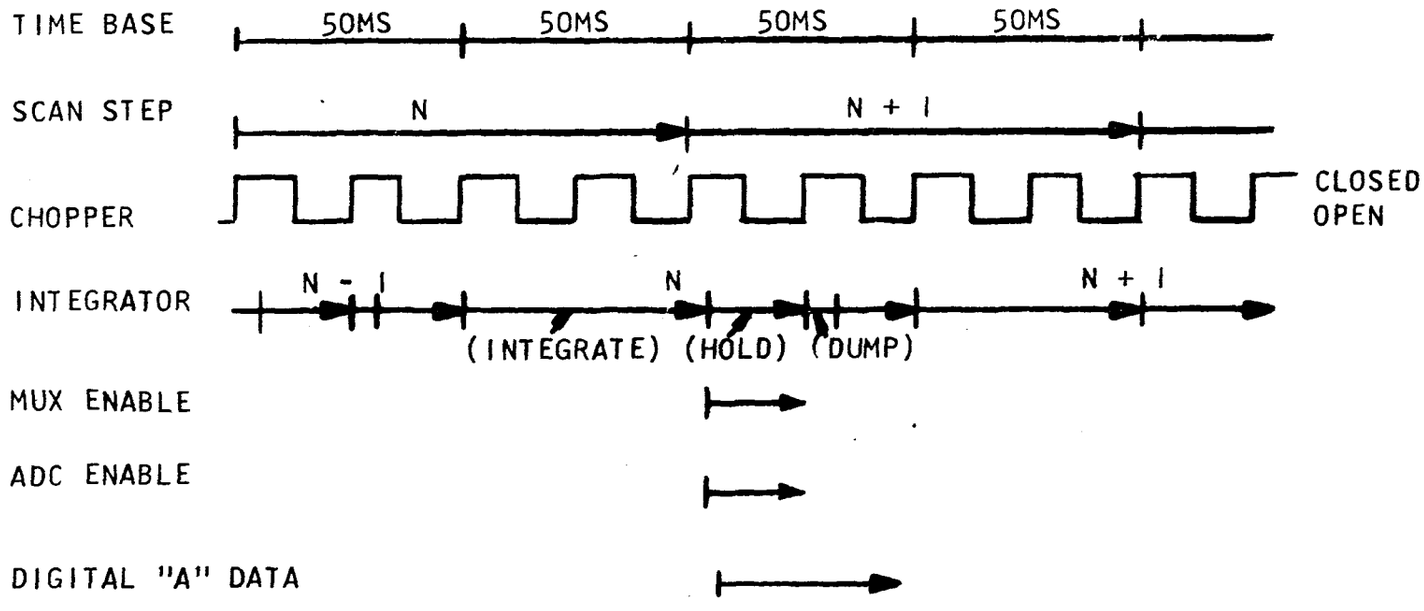


FIGURE A
TOVS SYSTEM TIMING

MULTIPLEXER CONTROL REQUIREMENTS

A logic configuration necessary to control the sequencing of the analog multiplexer is defined. Simple control digital circuitry is used to generate a fixed sampling sequence.

Multiplexer Review: A sequentially addressable, junction FET multiplexer is required to commutate the analog radiation signals, temperature monitor signals and other special analog voltages. A block diagram illustrating the multiplexer configuration is shown on the adjacent page. Note that control logic is required to provide the gate addresses for both the prime and submultiplexers.

Prime Multiplexer Control: The sixteen point prime multiplexer requires an address counter to sequentially scan the input gates. The two level nature of the multiplexer (4 x 4 matrix) allows a natural partition of a four (4) bit binary counter into two sets denoted as $SX_i/_1^4$ and $SY_i/_1^4$. These signals, when translated to compatible voltage levels, directly control the prime multiplexer.

Submultiplexer Control: Submultiplexer control is analogues to that used in the prime multiplexer, however, the twelve (12) point capacity require a different address counter radix. A twelve (12) state address counter is needed. This counter is advanced one count per FOV, or more correctly at a rate of 10 HZ. A data readout cycle is completed every 1.2 second period.

Synchronization: It is essential that the prime multiplexer address counter be synchronized to the TIP's major frame sync signal and the internal TOV's system timing. This requirement means that the address counters must be provided with a reset feature and that the advance rate maintain a fixed phase relationship to the integrate.

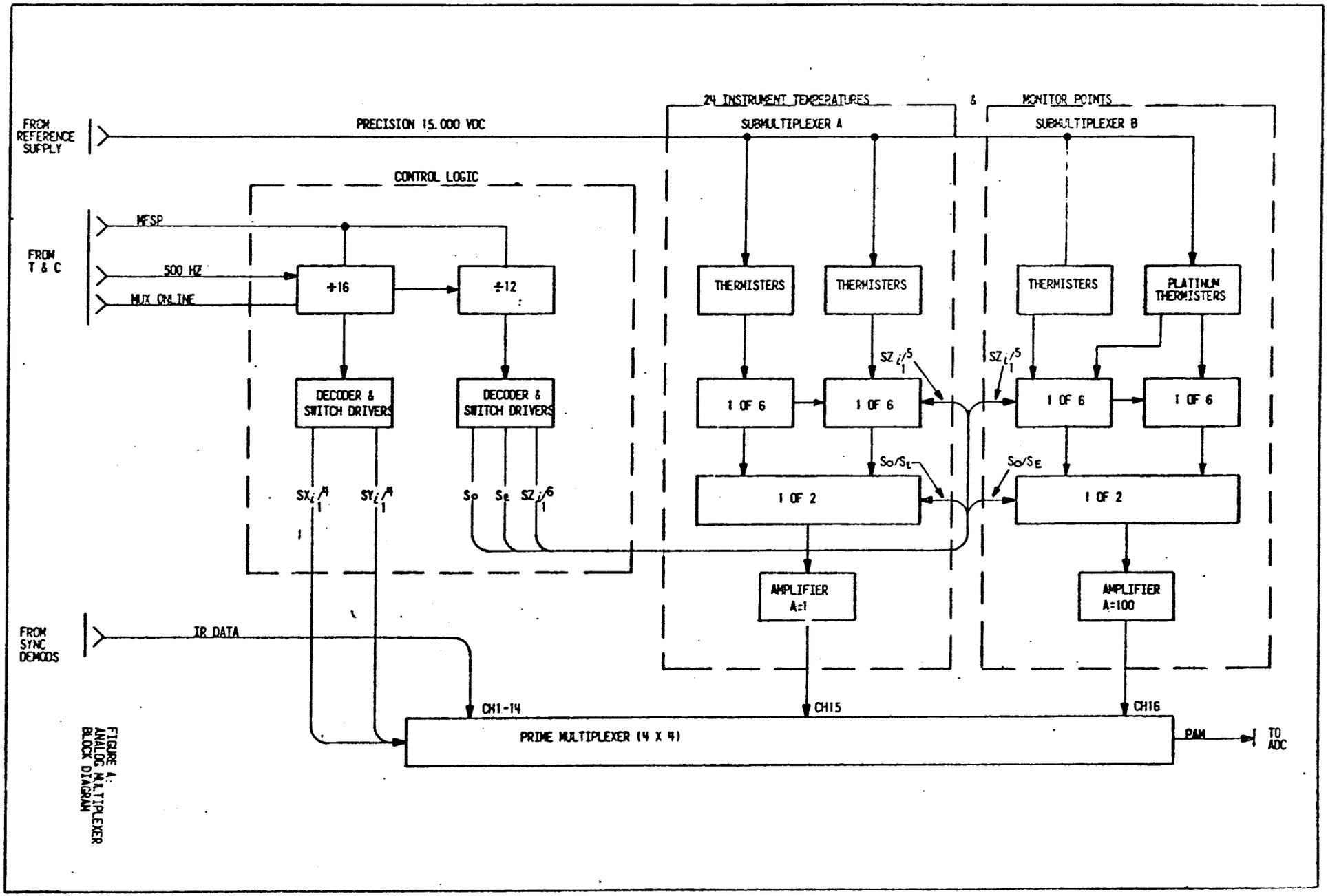


FIGURE 4: ANALOG MULTIPLEXER BLOCK DIAGRAM

DESCRIPTION OF THE MULTIPLEXER CONTROL LOGIC

Multiplexer control signals are developed using simple digital logic circuitry.

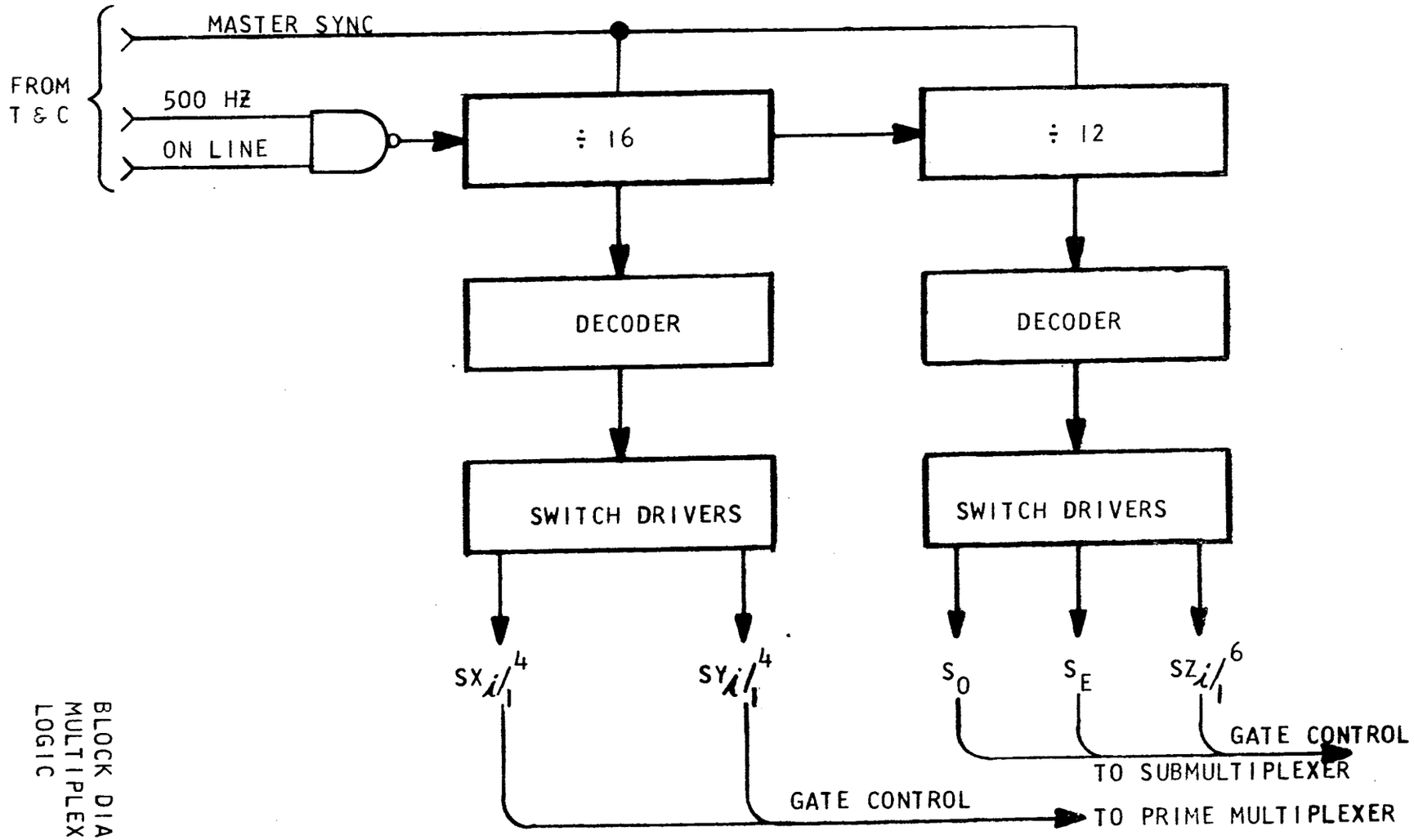
General: A simplified logic diagram of the multiplexer control logic is shown in Figure A and consists of prime and submultiplexer address counters, decoding gate and associated switch drivers.

Prime Multiplexer Control Logic: A four (4) bit binary counter is used to furnish the prime multiplexer address. Counter is advanced at a 500 HZ rate when the MUX ON LINE is enabled. Both of these signals are developed in the system timing and control unit, and function to rapidly step the prime multiplexer thru all 16 prime channels after the IR integration period. A reset feature is provided to synchronize the address counter to the TOV's system time. A signal denoted as MASTER SYNC accomplishes this objective.

Two input NAND gates are used to develop a 1 of 4 decoding network. Bits 2^0 and 2^1 form the control signals $SX_i/_1{}^4$; while bits 2^2 and 2^3 form control signals $SY_i/_1{}^4$. The SX_i and SY_i signals provide the matrix drive signal and when applied to 1st and 2nd level analog gates, select 1 of the 16 input gates.

Submultiplexer Control Logic: A divide by twelve counter is used to furnish the submultiplexer address. A two (2) stage configuration is suggested; i.e. a ÷ 2 stage and a ÷ 6 stage. A variety of configuration is available; however, the binary ÷ 2 coupled with a ÷ 6 shift counter yields an efficient decoding structure. The ÷ 2 stage supplies the SO,SE signals to control the 2nd level submultiplexer switches. The ÷ 6 shift counter is decoded into 1 of 6 active signals denoted as $SZ_i/_1{}^6$. Six (6) NAND gates (2 inputs/gate) are used to synthesize the decoder.

The submultiplexer address counter is advanced directly from the prime multiplexer address counter at a 10 HZ rate. Synchronization with the TOVs system time is assured via the reset action of the MASTER SYNC signal.



BLOCK DIAGRAM OF
MULTIPLEXER CONTROL
LOGIC

DESCRIPTION OF THE MULTIPLEXER TIMING

A timing diagram is presented to clarify the multiplexer control signal phase relationships.

General: A timing diagram illustrating the pulse duration and relative phase of multiplexer control signals are shown in Figures A and B. The MASTER SYNC signal, prime and submultiplexer address states, and matrix switch driver signals are identified.

Master Sync Signal: This signal occurs once every 256 seconds and provides the basic reference for the instrument. The leading edge of this 1 ms pulse is the time reference TO. This signal resets both address counters to zero.

Prime Multiplexer Address: The sixteen (16) states of the prime multiplexer address counter are identified. Each state is active for a 2 ms period during each multiplexer ON LINE cycle. This cycle occurs at a 10 HZ rate and is active for a 32 ms period.

The decoded counter states (SX_i and SY_i) are shown to illustrate the relative timing. Each SX_i signal is active for a 2 ms period every 8 ms. Each SY_i signal is active for an 8 ms period every 100 ms (once per FOV).

Submultiplexer Address: The twelve (12) states of the submultiplexer address counter are identified. Each state is active for a 100 ms period and is cyclic every 1.2 seconds.

The decoded switch driver signals are also shown. Signals So and Se correspond to the odd and even number of FOVs and are active for a 100 ms period every 200 ms. Signal SZ_i are active for 200 ms every 1.2 second.

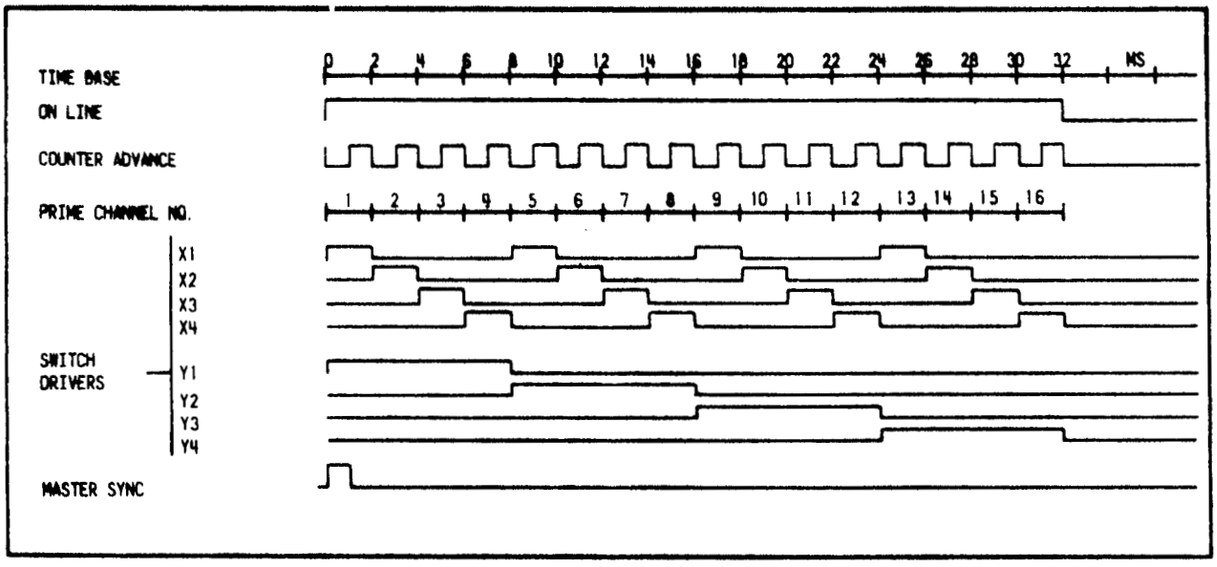


FIGURE A. PRIME MULTIPLEXER TIMING

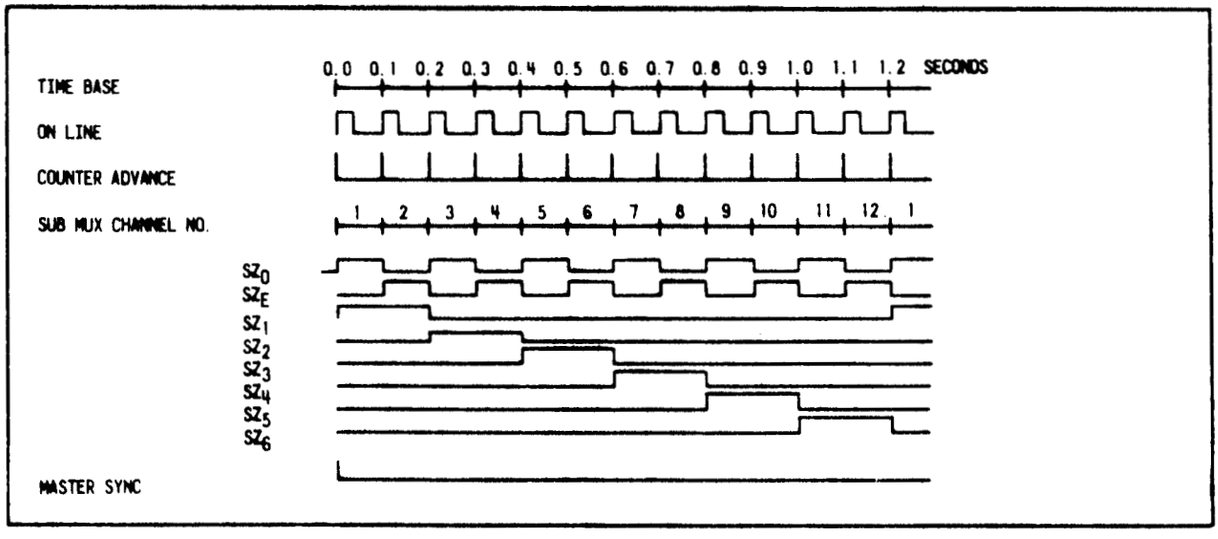


FIGURE B. SUBMULTIPLEXER TIMING

ADC CONTROL REQUIREMENTS

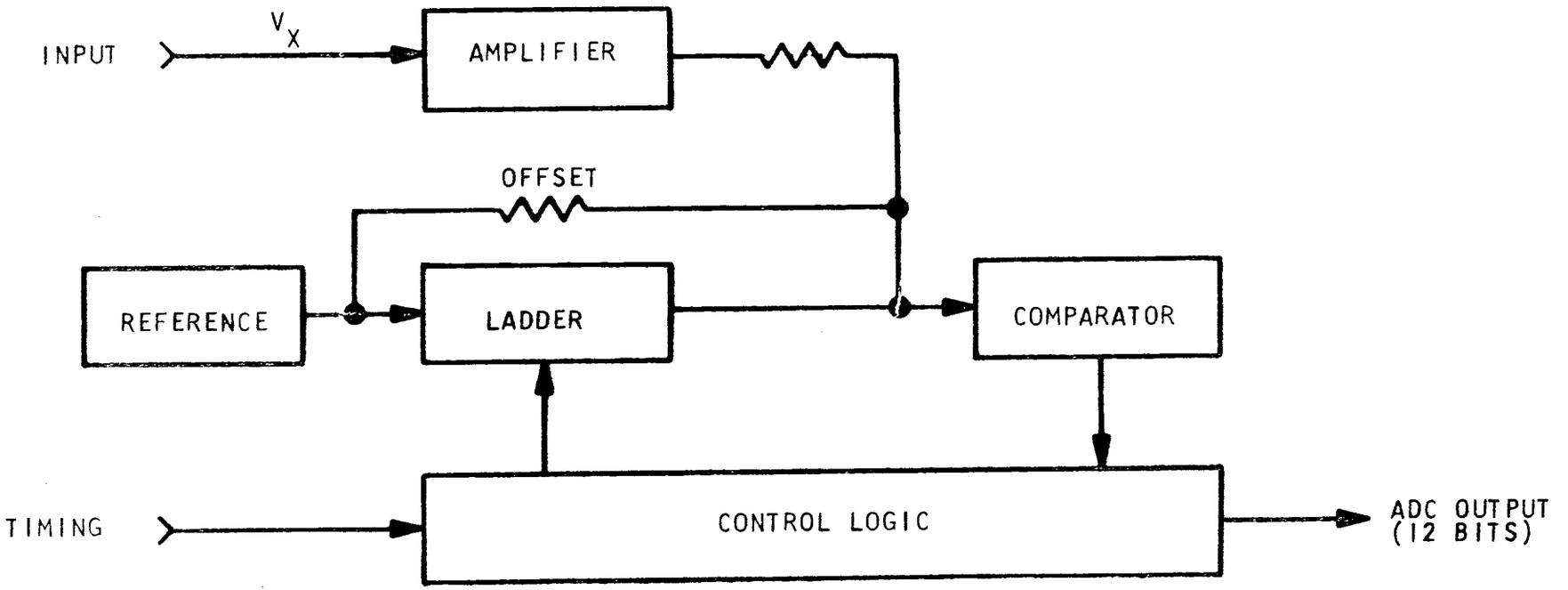
The signals necessary to control the analog to digital converter are identified. Circuit drive requirements and relative timing were considered.

Review of the ADC: A successive approximation, current summing, type of analog to digital converter is recommended for the TOVs. A block diagram illustrating the converter configuration is shown on the adjacent page. Note that logic circuitry is required to control the ladder network, store the partial results, output the digital data and start/stop the conversion process. These functions are performed by the control logic.

Start/Stop Conversion: A control signal obtained from the TOVs system timing and control unit is required to initiate the conversion process. Another signal generated within the control logic is required to denote that the quantization process is completed, and is identified as Conversion Complete signal.

Ladder Control: A twelve (12) bit current ladder is used to establish the binary weighted trail steps. Control requirements for this device can be stated as follows: first, each weighted binary bit must be applied sequentially for one bit period; second, the bit trail signal must be accepted or rejected based upon the decision of the comparator circuit.

Data Storage: A twelve (12) bit data register is required to accumulate the partial results obtained from each bit trail. This device functions in conjunction with the ladder control logic and also serves as a one (1) word buffer register to temporarily store the final encoded value.



SIMPLIFIED BLOCK DIAGRAM OF THE ADC

DESCRIPTION OF THE ADC CONTROL LOGIC

Control of the ADC is performed by well defined, simple, digital logic circuitry.

General: A simplified block diagram of the ADC control logic is shown on the adjacent page and consists of five functional elements. These functions must be performed, however several types of logic structures can be used to implement the control. The structure shown is similar to that employed on the ITPR. Alternate configurations were investigated, but none yielded significant advantages.

Start/Stop Control: The Start Conversion signal obtained from the system T & C unit is used to set the START/STOP flip-flop. This signal initializes the control logic to the state needed to start the conversion process. In particular it performs two functions; i.e., 1) resets the ADC register and 2) enables the trial counter. After the conversion is completed, the start/stop flip-flop is reset by the last trial ring.

Bit Trial Counter: A twelve (12) state counter and associated decoder are used to develop the bit trial signals. A two stage Johnston type shift counter (÷2 and ÷6), a single stage modulo-12 scaler, or a twelve state ring counter are suitable. The ring counter approach is the most simple to implement, however care must be exercised to insure that one and only one active state is possible.

Bit trial signals (T_i) are applied to the ladder driver gates and ADC register. Their purpose is to activate the appropriate ladder current switch and also to select the corresponding bit of the ADC register.

ADC Register: A twelve (12) bit register is used to store the partial results during the conversion cycle. RS, JK or D type logic elements can be used to construct the register; however, two basic capabilities must be provided, 1) a reset to zero capability, and 2) a conditional set based upon the logic AND function of the bit trial signal AND the ACCEPT/REJECT signal.

Register outputs are applied to the ladder driver gates to latch the bit trial steps and also serve as parallel digital data outputs from the ADC.

Comparator Strobe: An ACCEPT/REJECT signal is generated which denotes whether the bit currently being tried is too large or too small. The analog comparator output is gated with the trial clock to develop the desired signal. The exact circuit needed is dependent upon the nature of the ADC register, and can be a simple gate or at most a monostable multivibrator.

Ladder Drive Gates: Logic OR gates are required to control the current ladder switches. Twelve (12) gates of the two input type are needed. One input is furnished by the bit trial signals $T_i/_1^{12}$, while the other is supplied by the ADC register. This gating provides the conditional latching feature necessary to control each bit trial ladder switch.

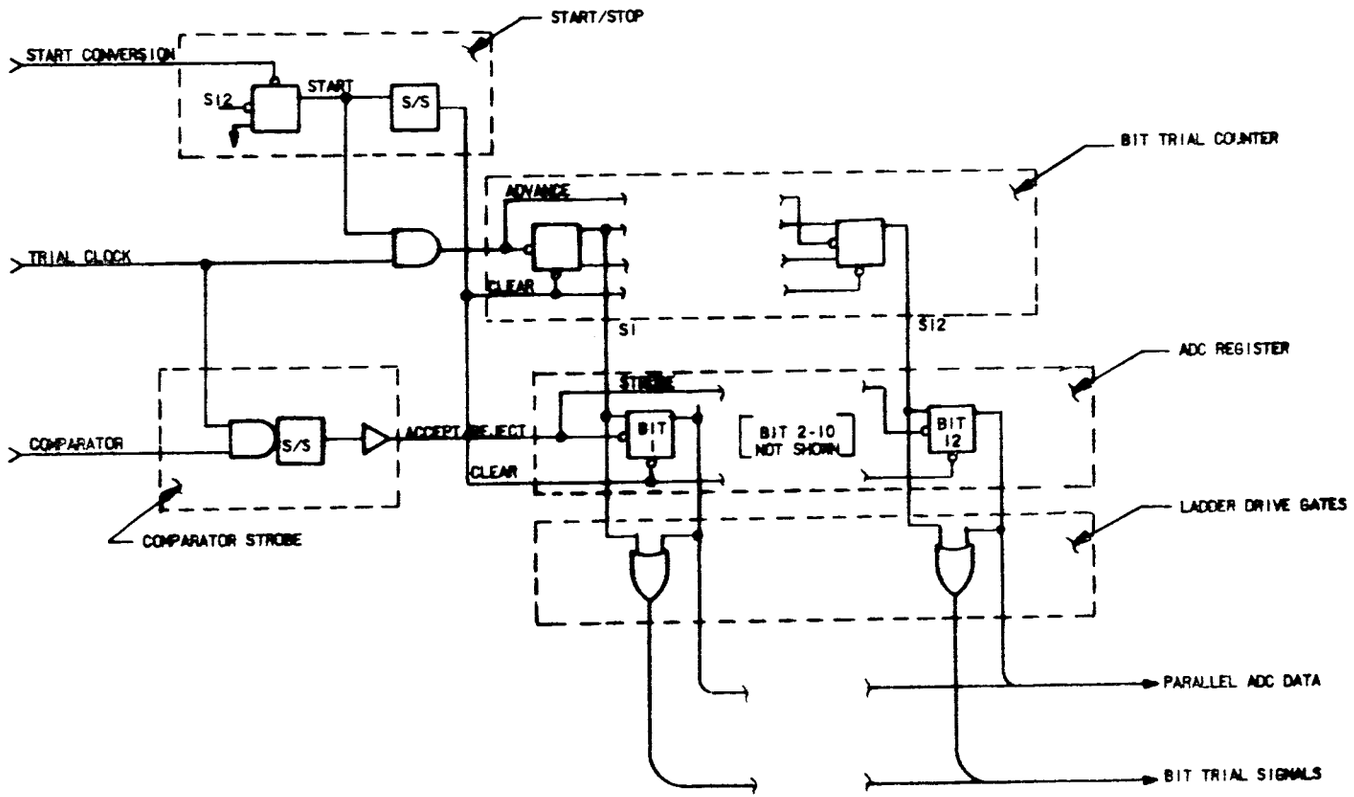


FIGURE A:
ADC CONTROL LOGIC

DESCRIPTION OF THE ADC TIMING

A timing diagram is generated and discussed to clarify the ADC control signal timing relationships.

General: A timing diagram illustrating the pulse duration and relative phase relationship of signals used to control the ADC is shown on the adjacent page. The trial clock, start conversion control, ADC register clear, bit trial signals, and conversion complete signals are shown.

Operation of the converter is initiated upon receipt of the START CONVERSION signal. This signal occurs at a 2.0 ms period. Pulse width characteristics are not critical and the duty cycle is optional. This signal will occur once for each analog sample to be digitized.

The CLEAR ADC REGISTER is derived from the leading edge of the START CONVERSION signal and is a 125 μs pulse.

Data Transfer Period: The time period corresponding to window number 16 (T_o + 1.875 thru T_o + 2.00 ms) is allocated for transfer of the ADC data to the formatter logic. Conversion process has been completed and the data is being held static and in parallel form. CONVERSION COMPLETE signal is used to control this transfer operation. This signal has a pulse width of 125 μseconds and occurs during window 16 time period.

A 375 μs period is allocated to permit the ADC and analog multiplexer to settle to a precision value. The bit trail signals start at time T_o + 0.25 ms and are complete by T_o + 1.875 ms. The encoded digital data is available for external use from T_o + 1.875 to T_o + 2.0 ms, at which time the cycle repeats.

Conversion Time: The conversion rate for the ADC has intentionally been kept at a slow rate to provide good accuracy at reasonable power. The basic rate is established by the number of data samples to be digitized during a fixed time interval. For the TOVS, sixteen (16) words must be encoded in 40 ms. This constraint, coupled with the output data rate of 500 HZ/word (max.) yields a range of conversion rates from 400 HZ to 500 HZ. The recommended conversion rates are as follows:

Word Conversion Rate .... 500 SPS (2ms/sample)
Bit Trial Rate .... 8 KHZ (125 μs/Bit)

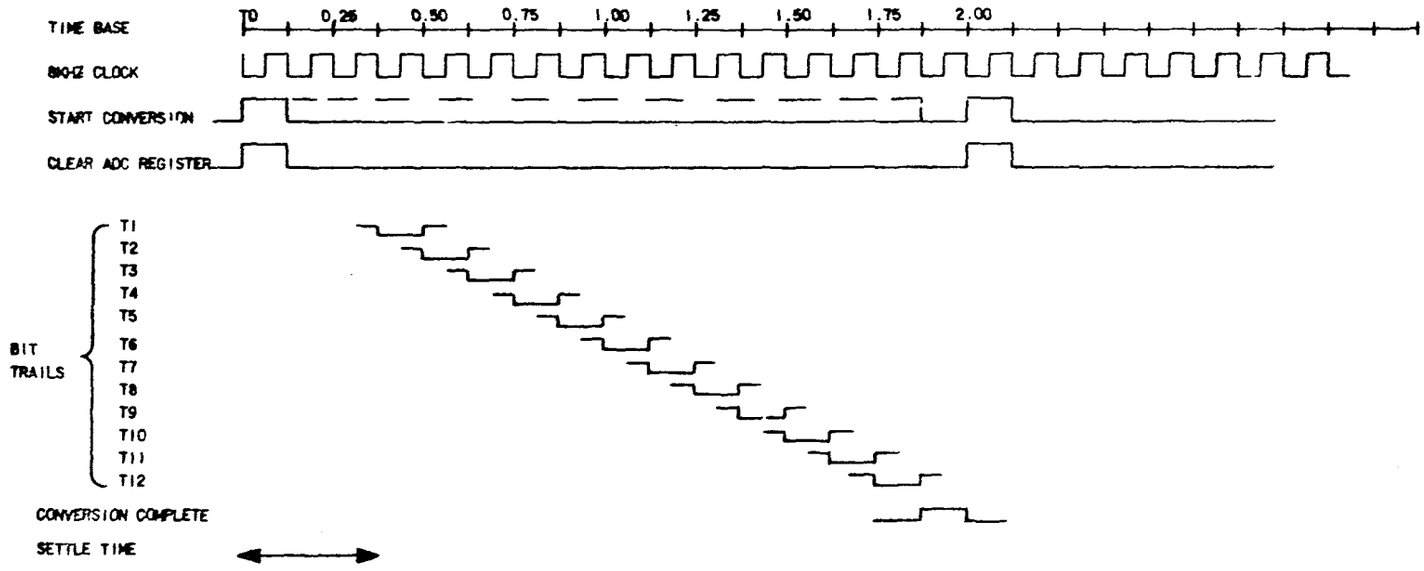


FIGURE A:
ADC TIMING DIAGRAM

EVALUATION OF SCAN MOTOR EXCITATION METHODS

A comparison of stepping motor excitation methods shows that the bipolar single-phase drive method provides a good torque output with moderate consumption and complexity.

Stepping motors provide discrete, incremental rotation in response to a pulsed input applied to the motor windings. Permanent-magnet stepping motors can be driven in several ways. The method for exciting the motor windings affects the efficiency, power consumption, speed, and torque characteristics. Five commonly used excitation techniques were evaluated: (1) unipolar, dual phase; (2) unipolar, single phase; (3) bipolar, dual phase; (4) bipolar, single phase; and (5) series, all windings. Unipolar techniques (1 and 2) provide current flow in one direction through the select excitation winding; while bipolar excitation provides current flow in both directions. Dual-phase excitation implies that two excitation phases are excited in parallel, while the single phase excitation methods excite only one coil or a series-connected coil.

Significant Characteristics of Excitation Methods - A tabulation of the five excitation methods is shown in the facing table. Power dissipation among the methods varies widely. Assuming Method 1 as a 100% reference, the relative power consumption is 100%, 70%, 50%, 35%, and 25% for Method 1 through 5, respectively.

Comparison of the ampere turns developed by each method affords a measure of the motor performance characteristics. Assuming Method 1 as a 100% reference, the relative values are 100%, 70%, 100%, 70% and 50% for Methods 1 through 5.

An efficiency factor is defined to relate the amount of power required per ampere turn (P/AT). The relative values are 1.4, 1.0, 0.7, 0.5 and 0.35 for Methods 1 through 5. Method 1 is the least efficient for convering power into usable ampere turns; while Method 5 is the most efficient.

Complexity of the drive circuitry required to synthesize the excitation methods was considered. The order is as follows; Method 2, 1, 4, 3 and 5, where Method 2 is the least complex.

Advantages and Disadvantages of Each Method - Method 1 (Unipolar, dual phase) develops the best motor characteristics, but at a high cost in power consumption. This method has the poorest conversion efficiency of all the methods.

Method 2 (Unipolar, single phase) develops good motor characteristics (similar to Method 4) at a reasonable power level. A very simple drive circuit can be used; in fact, this method is employed on the ITPR experiment. Power conversion efficiency is better than Method 1 but poorer than the other methods.

Method 3 (Bipolar, dual phase) develops the same motor characteristics as Method 1 at half the power. Power conversion efficiency is better than that of Methods 1 and 2, but poorer than that of the other methods. The drive circuit is more complex than either Methods 1, 2, or 4.

Method 4 (Bipolar, single phase) develops the same motor characteristics as Method 2 at half the power. Power conversion efficiency is better than that of all but Method 5. Drive circuit complexity is greater than either of the unipolar circuits; but not excessively complex.

Method 5 (all windings) dissipates the least circuit of power and provides the best power conversion efficiency, yet yields the poorest motor performance characteristics. A very complex drive circuit is required to produce the excitation sequence.

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Data System Division
R. G. Day

COMPARISON OF CANDIDATE MOTOR EXCITATION METHODS

Method	Method 1 Unipolar, Dual Phase	Method 2 Unipolar Single Ø	Method 3 Unipolar Dual Ø	Method 4 Bipolar Single Ø	Method 5 All Windings
Excitation Mode	(A+D) (A+C) (B+C) (B+D)	(A) (C) (B) (D)	(AB+CD) (AB+DC) (BA+DC) (BA+CD)	(AB) (CD) (BA) (DC)	(ABCD) (ABDC) (BADC) (BACD)
(A) Amp-Turns $A.T. = N_t N_t$	$I = \frac{V}{R}$ $\sum AT = NI\phi_1 + NI\phi_2$ $AT = \frac{1.4\ NV}{R}$	$I = \frac{V}{R}$ $\sum AT = \frac{NV}{R}$ $AT = \frac{NV}{R}$	$I = \frac{V}{2R}$ $\sum AT = \frac{2NV}{2R} + \frac{2NV}{2R}$ $AT = \frac{1.4\ NV}{R}$	$I = \frac{V}{2R}$ $\sum AT = \frac{2NV}{2R}$ $AT = \frac{NV}{R}$	$I = \frac{V}{4R}$ $\sum AT = \frac{2NV}{4R} + \frac{2NV}{4R}$ $AT = \frac{0.7\ NV}{R}$
(B) $\sum$ Power $P_t = V_t I_t$	$P_t = V\ I$ $P_t = \frac{2V^2}{R}$	$P_t = V_t I_t$ $P_t = \frac{V^2}{R}$	$P_t = V\ \frac{2V}{2R}$ $P_t = \frac{V^2}{R}$	$P_t = V_t I$ $P_t = \frac{V^2}{2R}$	$P_t = V_t I_t$ $P_t = \frac{V^2}{4R}$
(C) Eff. Factor	$F_1 = \frac{\frac{2V^2}{R}}{\frac{1.4\ NV}{R}}$ $F_1 = \frac{1.4\ V}{N}$	$F_2 = \frac{\frac{V^2}{R}}{\frac{NV}{R}}$ $F_2 = \frac{(1)\ V}{N}$	$F_3 = \frac{\frac{V^2}{R}}{\frac{1.4\ NV}{R}}$ $F_3 = \frac{(0.7)\ V}{N}$	$F_4 = \frac{\frac{V^2}{2R}}{\frac{NV}{R}}$ $F_4 = \frac{(0.5)\ V}{N}$	$F_5 = \frac{\frac{V^2}{4R}}{\frac{0.7\ NV}{R}}$ $F_5 = \frac{(0.35)\ V}{N}$
(D) % Power required Based on F_1 as 100%	Assumed 100% $\%P_1 = 100\%$	$\%\ P_2 = \frac{1.0}{1.4}$ $\%P_2 = 70\%$	$\%P_3 = \frac{0.7}{1.4}$ $\%P_3 = 50\%$	$\%P_4 = \frac{0.5}{1.4}$ $\%P_4 = 35\%$	$\%P_5 = \frac{0.35}{1.4}$ $\%P_5 = 25\%$

PERFORMANCE OF THE RECOMMENDED EXCITATION METHOD

The recommended bipolar single-phase drive method was used in the scanner breadboard and provided the torque needed to meet the retrace and 50 ms requirements with an acceptable power consumption.

Excitation Method 4 (Bipolar, single phase) is recommended for driving the BSU scan motor. A timing diagram illustrating the phasing of the four drive signals (A, B, C and D) is presented in Figure A. A simplified equivalent switching circuit is shown in Figure B. Note that the sequential closure (ground) of switches B, D, A, and C causes current flow through coils AB, CD, BA, and DC, respectively. Motor rotation direction is controlled by theorder of the sequence; i.e., BDAC for one direction, and CADB for the reverse direction.

Motor Response - Data obtained for an actual scan motor using Method 4 excitation verifies the low power consumption; however, the speed response was slightly less than anticipated. This characteristic is due primarily to the fact that the motor winding time constant is doubled in this configuration. Improvements in this characteristic are obtained by applying power for a longer duration.

Excitation for Retrace Cycle - During the retrace portion of the data scan, the motor excitation pulse width will be maintained at 10 ms and the stepping rate will be 100 pps. The breadboard scan mechanism was tested using this drive method to speeds of 115 pps.

Excitation Signals for Drive Cycle - During the data scan, the motor must step and settle within 50 ms, and the step rate must be 10 pps. Various excitation pulse widths and sequences were used to drive the scan mechanism in order to obtain an optimum value. An excitation time of 10 ms followed by a 20-ms off period and a 20-ms on period provided good speed, damping, and power performance characteristics.

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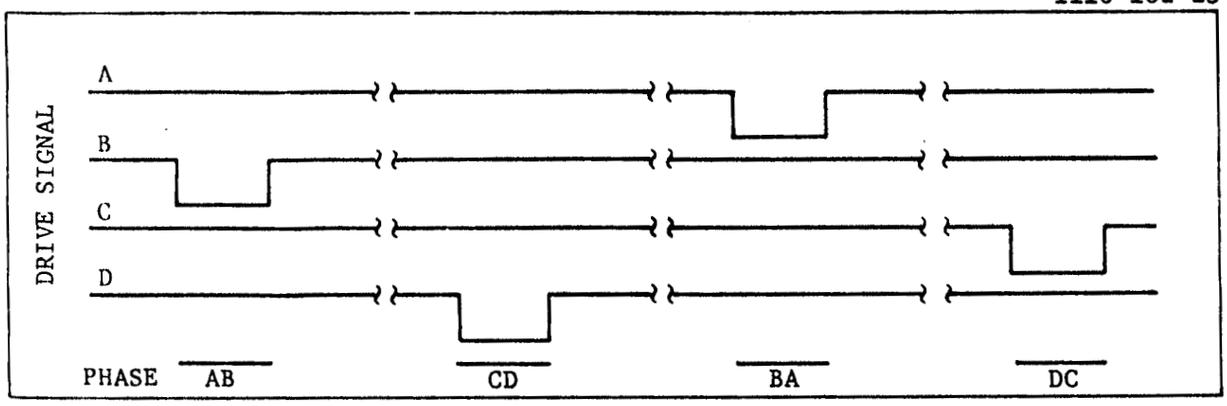

TIMING DIAGRAM FOR DRIVE SIGNALS

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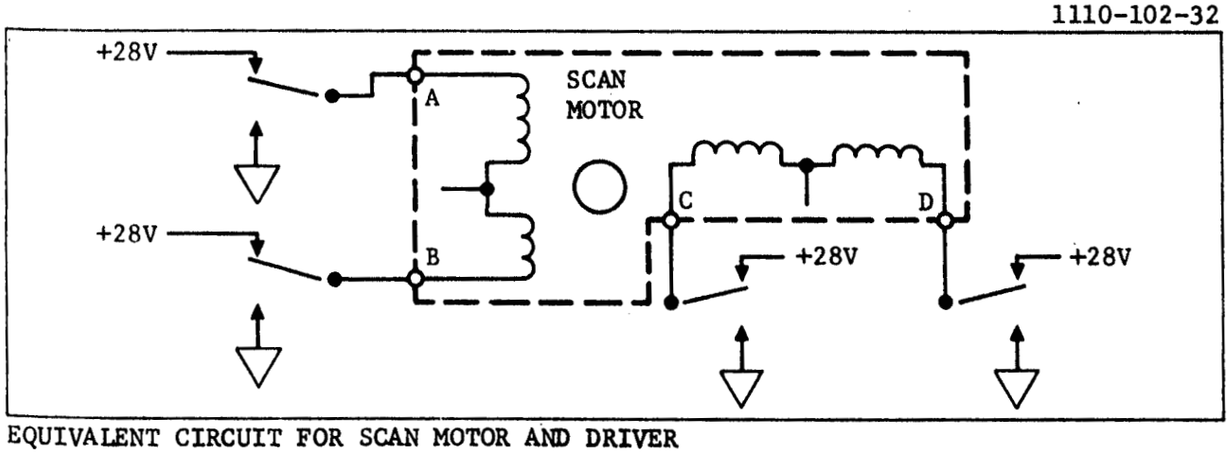

EQUIVALENT CIRCUIT FOR SCAN MOTOR AND DRIVER

DESCRIPTION OF SCAN LOGIC CIRCUIT

The logic required to generate the scan and retrace requires a position counter a two-bit up/down counter to select the motor phase, and a scan-retrace rate selection logic.

Scan Logic - A simplified block diagram of the scan logic is shown in the figure. Logic consists of five basic elements: (1) - 10 step-rate scaler, (2) step-rate selector switch, (3) - 72 position scaler, (4) up/down phase counter, and (5) direction control flip flop.

Circuitry used to synchronize the scan logic is not shown; nor is the logic used to position the scan mechanism at the blackbody or space position. These functions are omitted for clarity purposes; however, their implementation is a simple digital logic network.

Forward scan action is accomplished in 72 steps at a 100-ms step rate. Retrace is performed in a similar manner at a 10-ms step rate. Direction of scan is controlled by the four-state, up/down counter which generates the scan motor drive signal.

Position Counter - A 72-position counter is used to keep track of the FOV. A scan motor position encoder plus the TIP frame sync signal are used to initalize the - 72 scaler to the first FOV and set the scan mode flip flop to the forward direction.

The position counter is advanced one count per step. During the forward scan cycle, an advance rate of 10 pps is maintained until the position counter recycles from a count of 72 back to 0. This action sets the scan mode flip flop to the retrace position, and the advance rate is switched to 100 pps.

Scan Motor Drive Counter - A four-state, up/down counter generates the scan motor excitation signals A, B, C, and D. The direction of scan motor rotation is determined by the order in which the excitation signals are applied; i.e., forward scan requires the sequence BDAC, and retrace requires the sequence CADB.

The up/down counter generates precisely these sequences: where the UP mode corresponds to the forward scan and the DOWN mode corresponds to the retrace. The UP/DOWN mode is controlled directly from the Forward/Retrace flip flop.

Outputs from the UP/DOWN counter are gated with the position counter advance signals to develop the desired scan motor excitation pulse width. During the forward scan, a 30-ms pulse width is used, whereas a 10-ms pulse width is required during retrace.

Scan-Retrace Selector Logic - Selection logic is simply the AND/OR function, which is used to select the scan rate of 100 pps or 10 pps. The scan mode flip flop (Forward/Retrace) acts as the control signal. A prescaler ($\div$ 10) is employed to develop the 10 pps scan rate frequency directly from the 100 pps. This technique ensures that the proper phased signal is always available.

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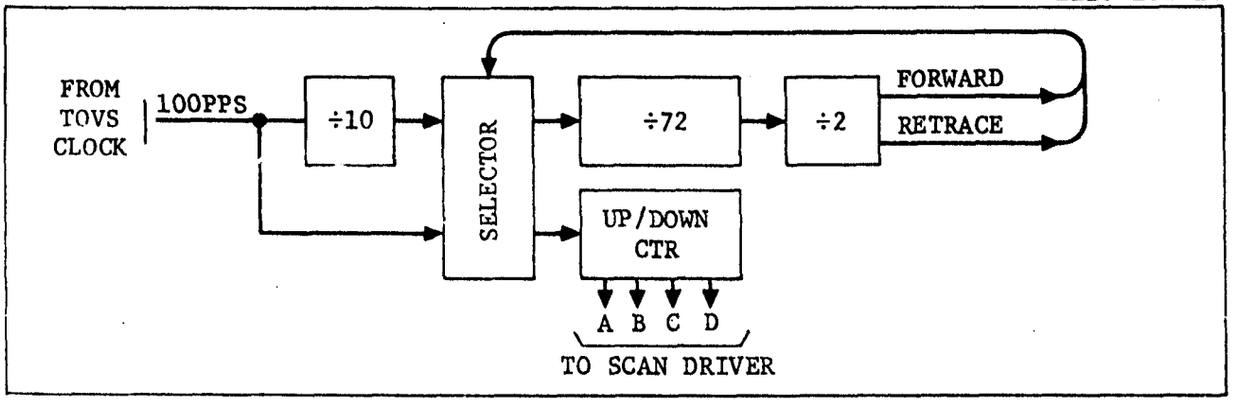

BLOCK DIAGRAM OF SCAN LOGIC

DESCRIPTION OF BREADBOARD DRIVE CIRCUIT

The drive circuit used for the scanner breadboard was a bridge circuit consisting of two complementary switches in a single-pole, double-throw configuration.

Drive Circuit - A drive circuit is required to interface between the scan motor and the scan motor logic. Requirements placed upon the scan motor drive circuit are as follows:

- Sink and supply 700 mA of current to an inductive load.
- Operate from a supply voltage (Vcc) of +28 Vdc.
- Dissipate low power during standby active periods.
- Compatible with low-power logic components.

The selected circuit which meets all these requirements is shown in the figure. Note that the circuit is complementary in nature and acts as a single-pole, double-throw switch, connecting either the 28-Vdc power or the ground bus to the output.

Circuit Description - The scan motor drive circuit uses a Darlington connection (Q1 & Q3) to achieve the high current gain required to buffer the low-power logic drive signal to the high current required by the load. A discrete transistor invertor stage (not shown) is used as a voltage gain to shift from logic levels (5 Vdc max.) to the 28-Vdc drive signal level. Output power transistor Q3 is protected from inductive overshoot by diode CR1. Associated biasing resistor values were selected for a worst-cast analysis. Note that the normal ON condition (output at 28V) is achieved, since the input at terminal (1) is normally near ground.

The lower section of the drive circuit uses an emitter-follower circuit (Q2) to drive the output power transistor (Q4) into saturation. Diode CR4 provides protection against the inductive overshoot. Capacitor C1 ensures that a break-before-make condition exists during turn ON. Input drive signal is obtained from the low-power logic.

A summary of the static transistor parameters illustrate the circuit capa capabilities:

Transistor	$(V_{CE})_{SAT}$,	h_{FE} @	$I_{C(mA)}$	P_D	V_{CEO}
2N2222A	0.3	100	150	0.5	50
2N2907A	0.4	100	150	0.4	60
2N5154	0.2	100	700	11.5	80

The basic power handling transistor is the 2N5154. This device is constructed using the double-diffused planar epitaxial process, and is well suited for this type of application.

Comparison With ITPR Circuit - The drive circuit used on ITPR was essentially a single-pole, single-throw switch used to apply -26 Vdc or open circuit to the output. Component redundancy (series and parallel) was employed for all current handling devices. The table opposite compares the BSU breadboard and ITPR characteristics.

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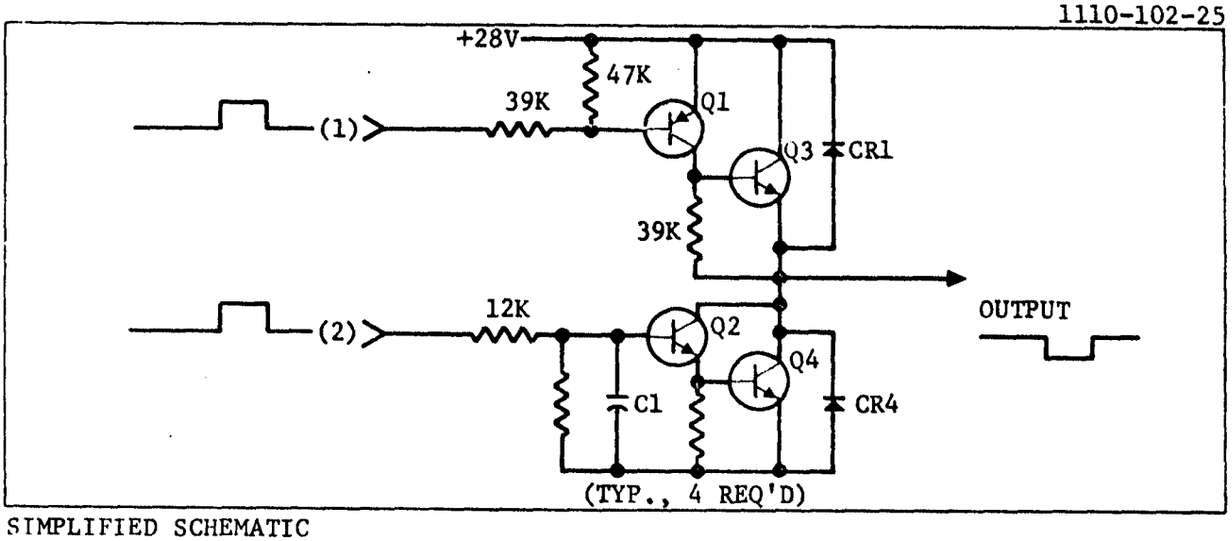
COMPARISON OF BSU BREADBOARD WITH ITPR

	ITPR	BSU Breadboard
Drive Method	Unipolar, Single Phase	Bipolar, Single Phase
Switch Type	SPST	SPDT
Load Current	-870 mA	±700 mA, peak
Component Redundancy	Yes	No
Max. Rep. Rate (retrace)	100 pps	100 pps
Power ON/step period	40 ms/400 ms	30 ms/100 ms
Duty Cycle	0.1	0.3
Peak Power	22.5 W	19.6 W
Power/Scan Step (average)	2.25 W	5.88 W
Operating Voltage	-26 Vdc	+28 Vdc
No. of Drivers Required	4	4



SIMPLIFIED SCHEMATIC
SCAN MOTOR DRIVE CIRCUIT

REDUNDANT DESIGN OF SCAN DRIVE CIRCUIT

Of the methods investigated to achieve component redundancy in the scan drive circuit, the series/parallel was selected because it works whether there is a short or an open component.

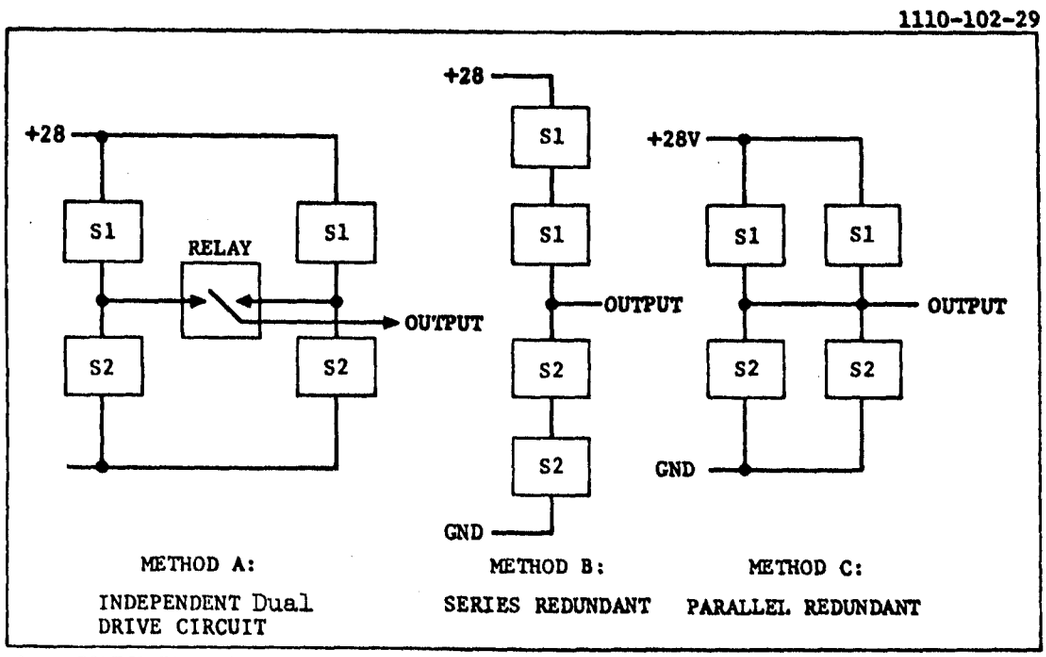
Component redundancy can be used to enhance the reliability of the drive circuit. Four types of component redundancy were considered:

Method A: Independent Dual Drive Circuits - A space craft command would be used to select the desired driver.
Method B: Series Redundant Drive Circuits - This circuit will operate properly for single-point failures which result in short circuits between collector and emitter.
Method C: Parallel Redundant Drive Circuit - This circuit will operate properly for single-point failures which result in open circuits between collector and emitter.
Method D: Series/Parallel Redundant Drive Circuit - This circuit will operate properly for single-point failures of either an open or short characteristic.

Figure A is a simplified switching diagram illustrating Methods A, B, and C. Method D is shown in Figure D. A ranking of circuit complexity is as follows:

(1) Least Complex: Method B & C
(2) More Complex: Method A
(3) Most Complex: Method D

Component redundancy Method D is recommended for the BSU scan drive circuit. An implementation of Method D (or B) is shown in Figure C.



A. COMPONENT REDUNDANCY METHODS.

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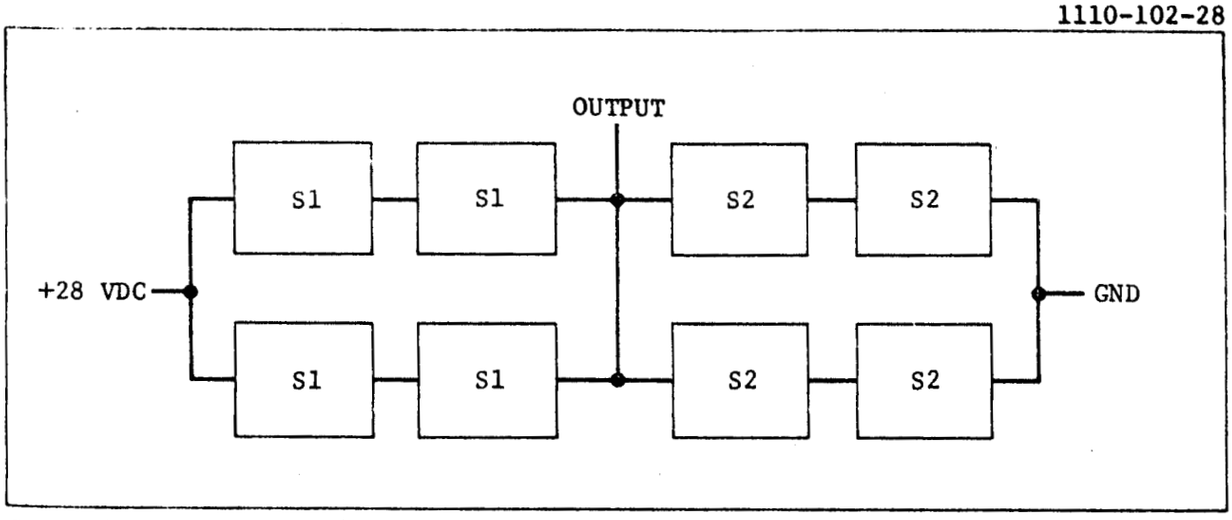

B. METHOD D: SERIES/PARALLEL REDUNDANT

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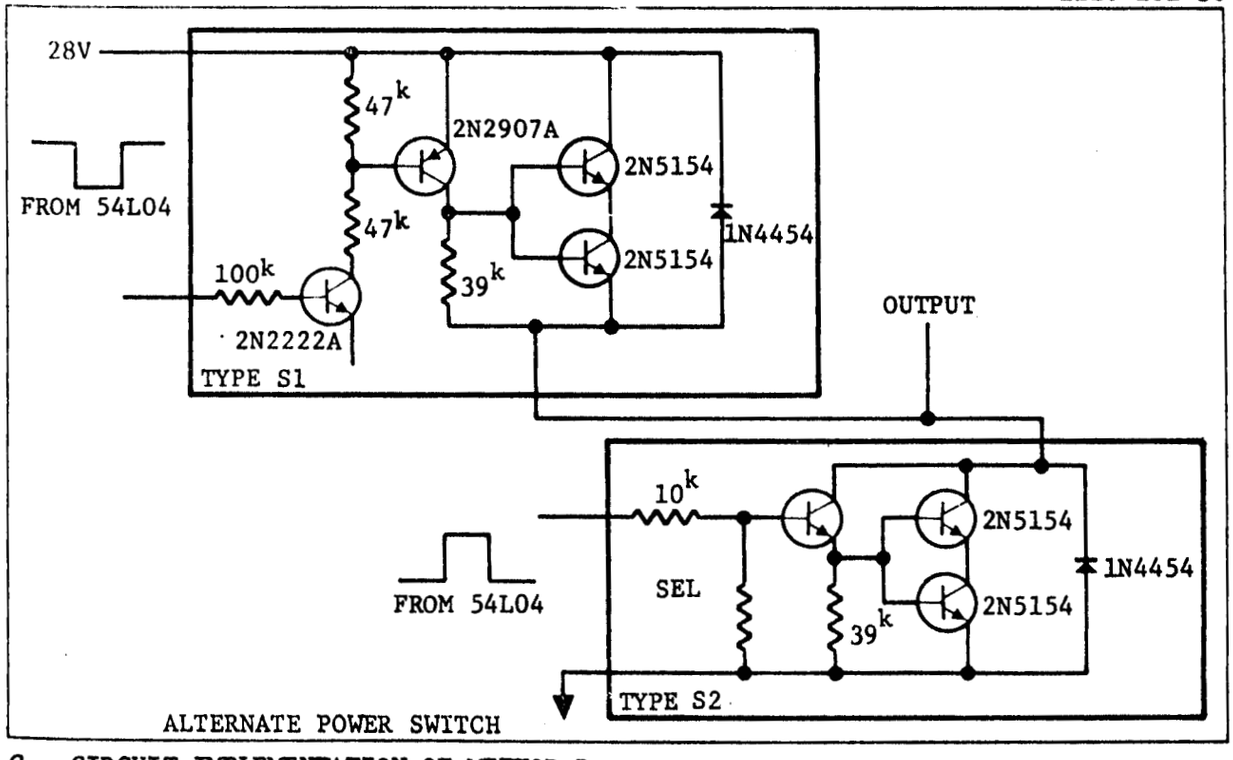

C. CIRCUIT IMPLEMENTATION OF METHOD D

ANALYSIS OF SCAN POWER REQUIREMENTS

The average power required by the scanner is 7.67 W, which because of power supply and drive circuit losses becomes 9.87W at the spacecraft bus. The transient load during step and retrace because of its size and low frequency content, cannot be filtered effectively and will be reflected to the spacecraft.

Power Requirements - Power is dissipated in three (3) functional elements; i.e. 1) scan motor windings, 2) motor excitation drive circuits, and 3) scan mechanism control logic.

Power required to drive Compute Devices motor, Model 15P03 can be computed as a worst case value from $V^2/2R$; where V = 28 V and R = 20 . Secondary effects of back emf and inductance are neglected in order to obtain a limiting value. Peak power dissipated within the motor coil is 19.6 watts.

Power losses within the motor excitation drive circuit amounts to 1.7 W, maximum, peak instantaneous. This loss is due primarily to the motor excitation current flowing through the output driver transistors.

Scan motor control logic dissipates approximately 0.20 W. This is a constant power drain required to keep the scan motor logic active at all times.

Power Dissipation per Cycle - A duty cycle factor is applied to compute the average power required per step; since scan motor power is applied for only 30 msec/step during the scan mode and 10 ms/step during the retrace mode.

The duty cycle factor for the combined scan/retrace cycle is 0.36. This number was obtained from this ratio:

T_1/T_2 where:

T_1 = total time power is applied to motor (2.88 sec)

T_2 = scan/retrace period (8.00 sec)

The average power dissipated per scan/retrace cycle is 7.67 W. A plot of the average power versus time is shown in the visual plan as Figure A.

The power profile required to complete the entire scan cycle (data plus calibration) is shown in Figure B. Thirty-one (31) scan retrace cycles, plus one calibration cycles are completed on a 256 second period. Average power for scan and retrace is 7.67 W, while the average dissipation during the calibration interval is 8.53 W. Combining these values yield as a total of 7.70 W average for the entire scan mechanism and drive circuit.

TOVS BSU Power Supply Effects - TOVS power supply efficiency will effect the actual input power required to drive the scan mechanism. Peak power loads will be directly reflected as current demands from the primary spacecraft power system. Assuming a power conversion efficiency of 78% including drive circuit losses yields an input power of 9.87 W, average. The peak requirements is 27.3 W for as long as 1.24 sec. during the scan return from housing calibration.

Very little power smoothing (averaging) will occur since the power supply filters do not afford sufficient energy storage. Hence, the total load power requirement is reflected directly upon the s/c battery.

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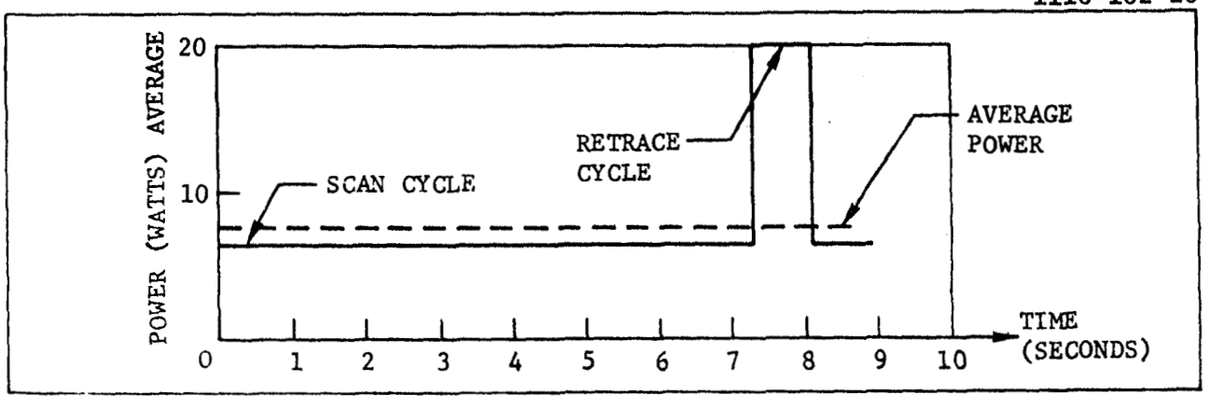

FIGURE A. POWER PROFILE FOR SCAN/RETRACE CYCLE

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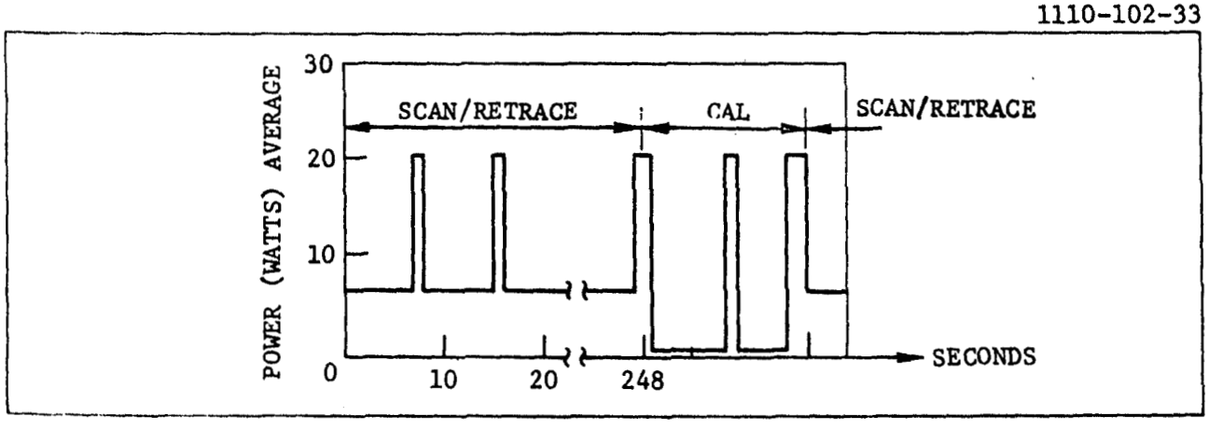


FIGURE B. POWER PROFILE FOR DATA/CAL CYCLE

CHOPPER MOTOR AND EXCITATION METHOD

An A/C synchronous motor driven from a constraint frequency excitation source is recommended as the optical chopper power source.

General: An A/C synchronous motor operates at a constant speed which is independent of the load, but directly proportional to the excitation frequency. This motor can be driven with either a sinusodial or square wave excitation wave form.

Excitation Methods: A two (2) phase excitation signal is required. The signals can be either AC or DC, but they must be 90° out of phase and provide current flow in both directions thru the windings. Four (4) methods were considered:

Method 1: AC, single phase
Method 2: AC, dual phase
Method 3: DC, single phase
Method 4: DC, dual phase

Methods 1 and 2 dissipate the least power within the motor, but requires sinusoidal type drive signals and linear power drive amplifiers. Power savings in the motor are cancelled by the linear power amplifier dissipation and complexity of the sine wave generating circuitry.

Methods 3 and 4 use square wave signals for the motor control. Method 3 uses a single excitation drive and provides a 90° passive phase shift network to develop the other phase.

Recommended Excitation Method: Method 4 is the drive technique used on ITPR and is the recommended approach for the TOV's. This recommendation is based on the simple drive circuit employed, relatively low power consumption, and demonstrated operational performance.

Drive Signal Description: A timing diagram illustrating the phasing of the four drive signals ($\phi 1$, $\phi 2$, $\overline{\phi 1}$, $\overline{\phi 2}$) plus a simplified equivalent switching circuit is shown in the Figure on the adjacent page. Note that signals $\phi 1$ and $\overline{\phi 1}$ are 180° out of phase, causing bidirectional current flow. In like manner, $\phi 2$ and $\overline{\phi 2}$ control the Phase 2 winding. Also note that $\phi 1$ and $\overline{\phi 2}$ are 90° out of phase.

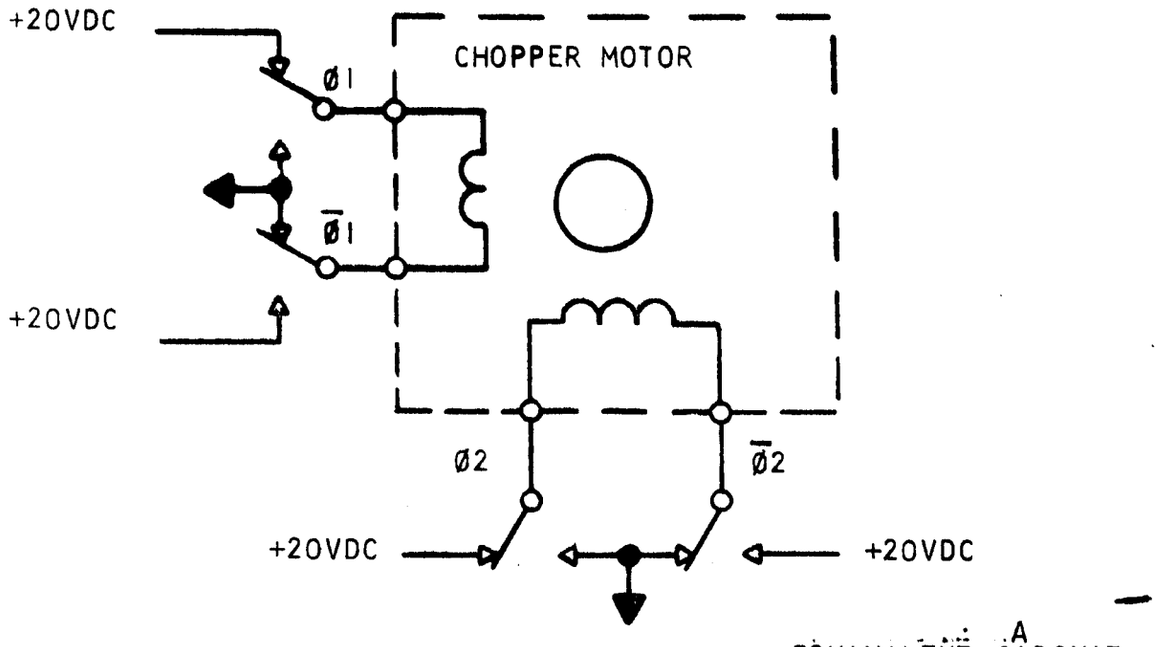
Chopper Motor Drive Circuit: A power switch is required to drive the chopper motor coils. Circuit must be capable of supplying and sinking current (100 mA) to an inductive load.

The bridge type driver circuit used on the scan motor driver is recommended.

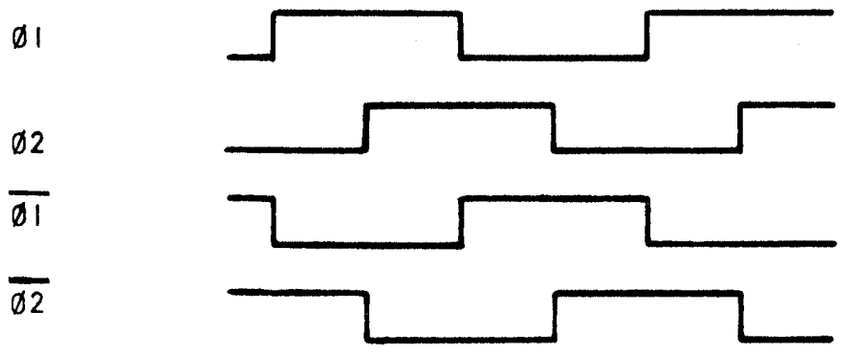
Power Requirements: Power is dissipated in three (3) areas; i.e., 1) chopper motor windings, 2) excitation drive circuit, and 3) control logic. The power consumption is as follows:

Motor Windings:	2.75 watts
Drive Circuit:	0.35 watts
Control Logic:	0.15 watts
Total:	3.25 watts, maximum

The power profile is essentially constant, except for a transient which occurs at the driving frequency. The power transient is of short duration, 10 to 20 μs, and occurs when the excitation signal changes states.



EQUIVALENT CIRCUIT
CHOPPER MOTOR &
DRIVER



TIMING DIAGRAM
EXCITATION SIGNALS

PHASE CONTROL OF THE CHOPPER MOTOR

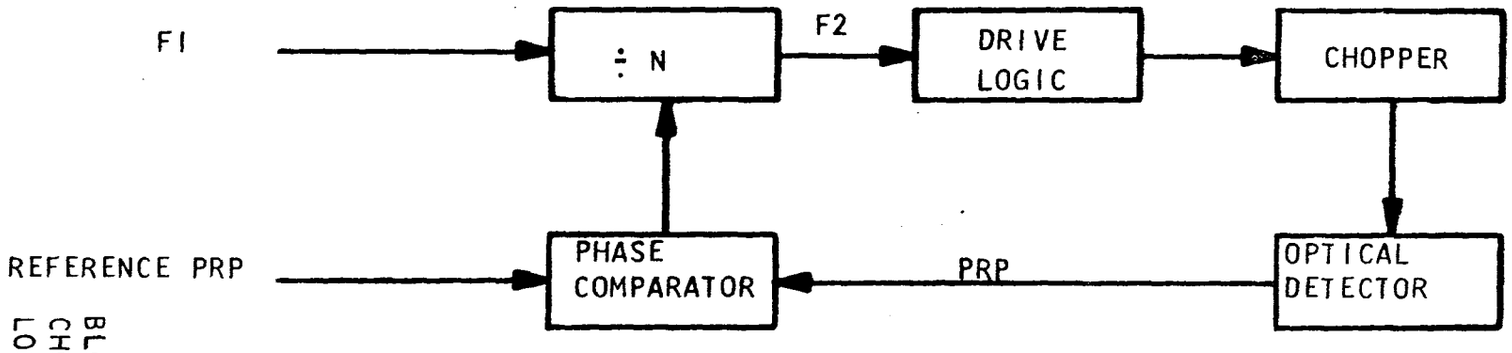
A digital phase locked loop is recommended as the means for controlling the chopper motor phase.

Requirement: Due to the limited number of chopper cycles occurring during the dwell period, it is essential that the chopper motor be phase locked to the infrared energy integrator control. This interlock will assure that the integration is synchronized and phased with the basic TOVS system timing, thus tying together the step scan, integration, sampling and digitization processes.

Configuration: A block diagram illustrating the digital phase locked loop is shown in Figure A on the adjacent page. Five (5) functional elements comprise the circuit. A brief description of each elements is as follows:

- Chopper - An optical chopper mechanism powered by an A/C synchronous motor.
- Optical Detector - A circuit used to determine the phase of the chopper wheel, via a light emitting diode and associated detector.
- Phase Comparator - A digital circuit used to determine the phase difference between the electrical PRP reference signal and the actual PRP.
- ÷ N Scaler - A variable length counter used to adjust the drive frequency by I:100 from the nominal value.
- Drive Logic - A digital network which conditions the frequency F2 to drive the chopper motor.

Operation: The loop functions to keep the PRP signal (obtained optically via the mechanical chopper) in phase with the chopper reference clock which is obtained directly from the TOVS system clock. This is accomplished by the action of the variable modulous divider and phase comparator.



BLOCK DIAGRAM
CHOPPER SYNCHRONIZATION
LOGIC

DUAL INSTRUMENT MODE CONTROL DESCRIPTION

A special operating mode utilizing two (2) TOVs instruments was studied to determine the support requirements when data is obtained from both instruments.

General: Operating conditions required during this mode are summarized below:

a) A unique S/C command will be used to identify the dual operating mode.
b) Both TOVS instruments A and B will be powered and conditioned to gather data at one-half the normal rate.
c) Both TOVS instruments will be controlled to obtain data from the same field of view; $(FOV)_a \equiv (FOV)_b$.
d) TOVS data readout will be performed in the normal manner; i.e., as commanded by the TIP control signals but at a reduced rate.
e) Effective scan rate of TOVS instruments A and B will be reduced to one-half (1/2) the original scan rate to allow the TIP system to maintain its normal data rate.

A simplified block diagram illustrating the relationships of the major subsystems is shown in Figure A. Note that a single S/C command is applied to both $(TOV)_a$, $(TOV)_b$ and TIP to initiate the dual mode operation, also that the TOVS outputs are dedicated to unique TIP channels.

Support Requirements: Dual instrument operating mode imposes requirements upon several spacecraft subsystems including the TOVS, TIP, S/C Command and S/C Power systems. The requirements are listed below:

a) TOVS System: Provide the capabilities described above.
b) TIP System: Provide the data processing capability necessary to alternately address each TOVs instrument.
c) S/C Command System: Provide an unique command to identify the dual instrument mode.
d) Power System: Provide sufficient power to sustain a dual instrument operation. Approximately 55 watts is required to support TOVS A and B during the dual mode.

Scan Mechanism Control: Two (2) major control functions performed by the scan mechanism logic should be provided; i.e.,

a) Scan rate should be reduced from 100 ms/step to 200 ms/step for TOVS A and B.
b) Scan position counters must be synchronized to the same FOV.

One method of implementing these control functions is discussed below. Note that the control function is entirely digital in nature and is a simple logic selection process controlled by the S/C Dual Instrument Command.

Scan Rate Control: A simplified block diagram of the scan logic is shown in Figure A and a timing diagram in Figure B.

Scan rate is selected via the AND/OR logic, as 100 ms/step (normal scan mode) or 200 ms/step (dual instrument mode). A second AND/OR selection network is required for the retrace rates of 10 ms/step and 20 ms/step. Since all the instrument timing signals are derived directly from the S/C clock via digital scalers, the stepping rates for $(TOV)_a$ and $(TOV)_b$ are identical in frequency.

Scan Position Synchronism: A time reference marker is required to synchronize the position address counters for both TOVS A and B.

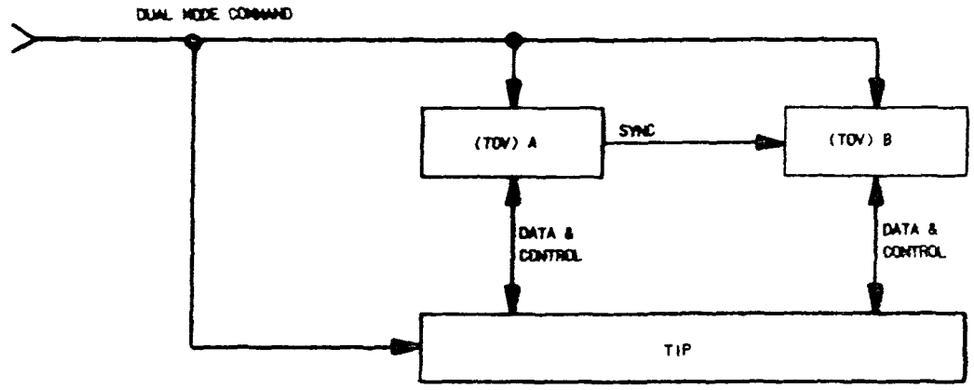


FIGURE A:
BLOCK DIAGRAM OF THE DUAL INSTRUMENT MODE

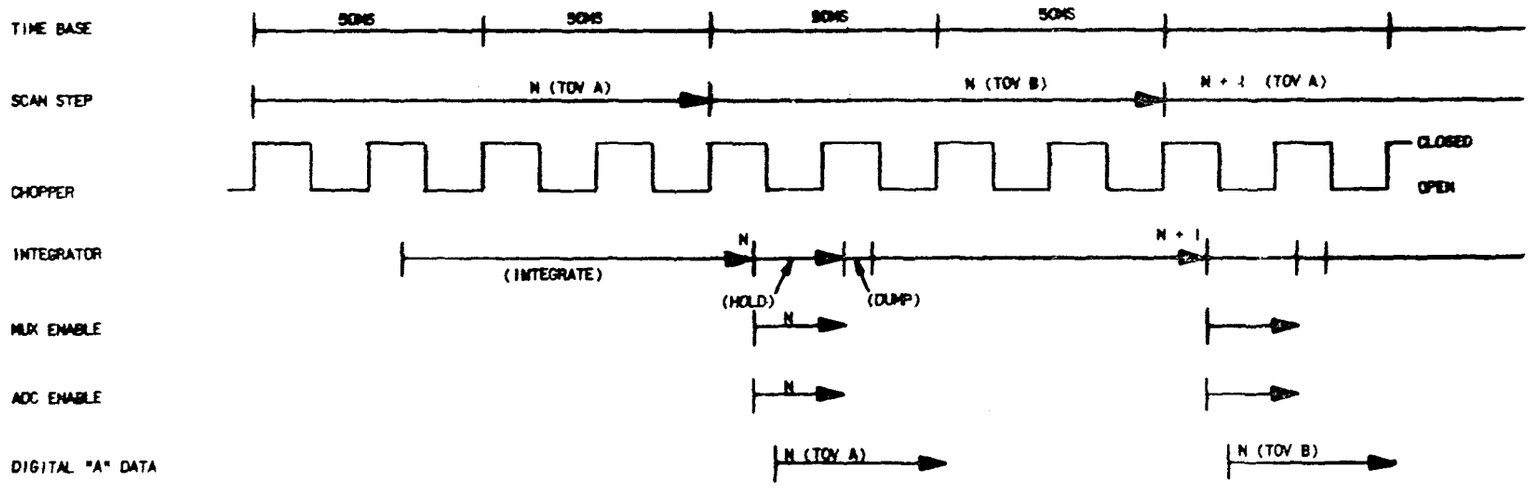


FIGURE B:
DUAL INSTRUMENT TIMING

FORMATTING UNIT DESCRIPTION

Logic circuitry necessary to control the transfer of data from the TOVS instrument to the S/C telemetry information processor is defined. This logic is defined as the Formatting unit.

Data Output Form: All critical data is supplied in serial digital form, similar to NIMBUS digital "A". This data form is recommended to allow the TOVS to use its interval 12-bit ADC in lieu of the TIPs 8-bit converter. Interface signals between the TIP and TOVS are assumed to be similar to those supplied by the VIP.

Buffer Requirements: Interfacing the TOVS instrument with an external data processor was considered from two viewpoints, i.e.,

1) What is the most hardware efficient interface? and
2) What is the most flexible type of interface?

The answer is basically, how much temporary buffer storage is supplied. A minimum of a one (1) word buffer register (16 bits) is necessary and represents the most efficient hardware interface; yet it provides the most strigent requirement on the S/C data processor.

A comparison of three possible interface configurations was conducted and is presented in Table A.

Configuration Description: A simplified block diagram of the formatter unit is shown in Figure B, and illustrates the Method 1 configuration. Methods 2 and 3 are similar, except that the one (1) word buffer register is expanded to a sixteen (16) word capacity.

Logic gates digitally multiplex the data into the storage register, which also acts as a parallel to serial converter. Parity is generated in a serial manner and inserted into the data bit stream via the output selection gates.

ITEM	METHOD 1	METHOD 2	METHOD 3
BUFFER TYPE	Interlaced Load/Unload	Non-Interlaced Load/Unload	Interlaced Load/Unload
CAPACITY	1 Word (16 Bits)	16 Words (256 Bits)	16 Words (256 Bits)
FLEXIBILITY	Least Flexible	More Flexible	Most Flexible
RESTRICTIONS	(1) Requires TOVS and TIP Formats to be synchronized. (2) Requires that 14 TIP Words (adjacent) be readout at a rate of 1 word/2 ms (500 HZ). Readout period is fixed.	(1) Requires that TOVS and TIP Formats to be synchronized. (2) Requires that TOVS Data (16 Words) be readout at any time during a fixed 75 ms period.	(1) Requires that TOVS Data (16 Words) be readout at any time during a 100 ms period
COMPLEXITY	Least Complex	More Complex	Most Complex
VOLUMN ESTIMATE	1.0 (Reference)	1.8	2.0
POWER ESTIMATE	1.0 (Reference)	1.0	1.2
WEIGHT ESTIMATE	1.0 (Reference)	1.1	1.2
AVAILABLE PARTS	(1) Flip-flop register using 54L or CMOS	(1) Multiple register per Method 1. (2) CMOS RAM (3) PMOS RAM (4) PMOS Shift Register	Same as Method 2

TABLE A: BUFFER COMPARISON TABLE

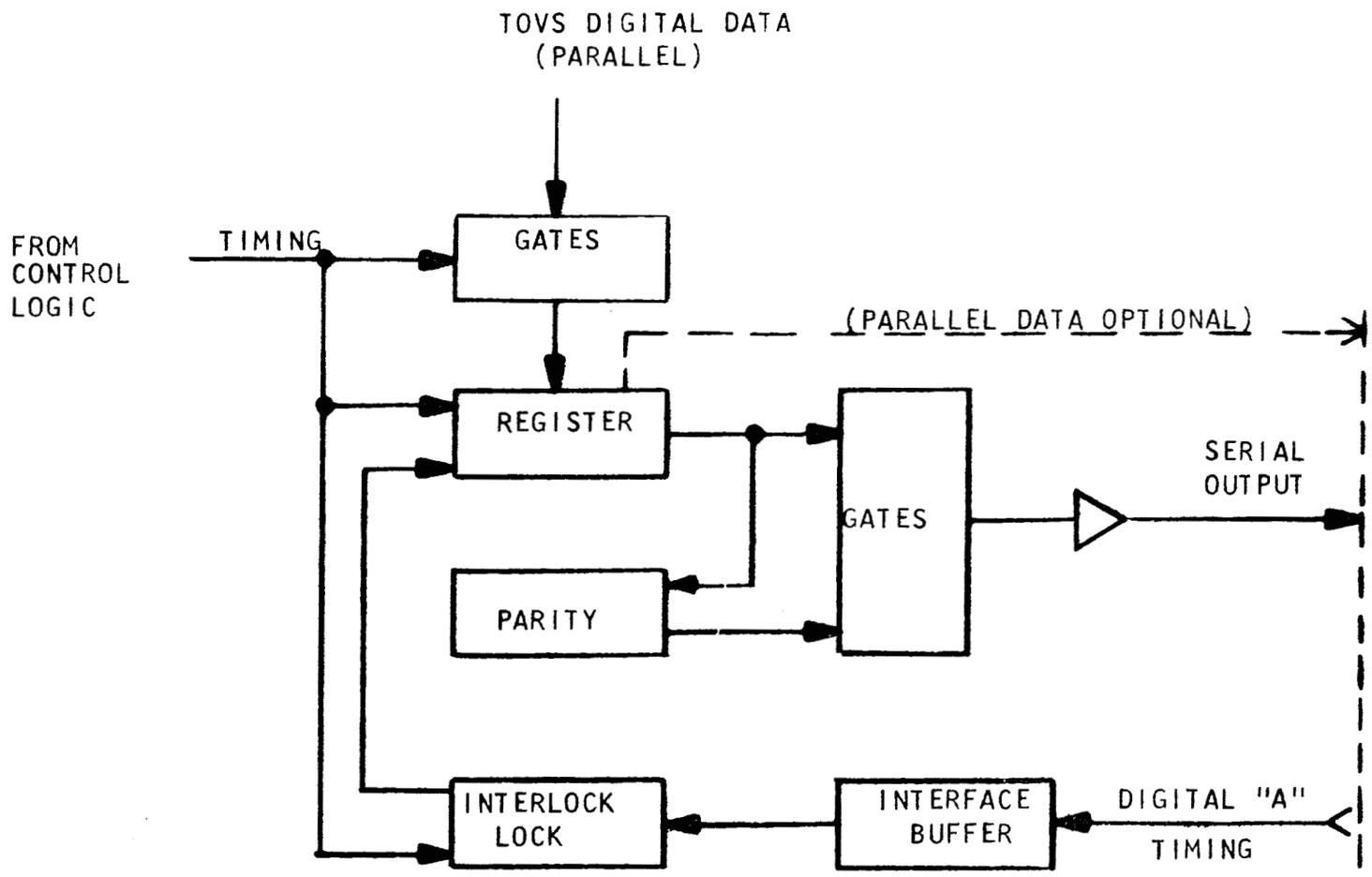


FIGURE B
BLOCK DIAGRAM OF
THE OUTPUT
FORMATTER

DATA FORMAT

The data word length, structure and contents are identified. Data which supports the primary infrared energy measurement is included.

Word Format: A suggested word format diagram is shown in Figure A. The TOVS word is sixteen (16) bits. The word is divided into two (2) fields; Field A consists of bits 9 thru 16 and Field B consists of bits 1 thru 8. Field A bits would be located in TIP word slot N and Field B bits would be packed into word slots N + 1.

A word parity bit is generated and located in bit Position 1. Odd parity is employed.

Bit positions 2, 3 and 4 are used for monitor flags and position data. Recommended discrete bits are tabulated in Figure B.

Bit positions 5 thru 16 are allocated for the digital value of the measurement; where bit 5 is the LSB, bit 14 is the MSB and bit 16 is the sign.

BITS POSITION

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
P	X	X	X	0	1	2	3	4	5	6	7	8	9	10	S

TOVS DATA

DISCRETE BITS

PARITY

NOTE:
1. TIP Word N, Bits 9 thru 16, TOVS Word Y
   TIP Word N + 1, Bits 1 thru 8, TOVS Word Y
2. 16 TOVS words will be used to process data from 1 FOV
3. 48 bits of discrete data will be inserted into the X X X bit position (See Figure B)
4. Bit position 16 is the MSB and will be shifted to the TIP as the 1st bit.
5. Bit position 1 is the parity bit for the 16 bit TOVS word.

FIGURE A: TOVS WORDS FORMAT

MONITOR	NO. OF BITS
Shaft Angle Encoder	7
FOV Electrical Address	7
Line Number Counter	8
Position Flag P1, Nadir	1
Position Flag P2, Housing	1
Position Flag P3, Space	1
Mode Flag M1, Earth Scan	1
Mode Flag M2, IR Cal.	1
Mode Flag M3, Electrical Cal.	1
Mode Flag M4, Dual Mode	1
PRP Operating Flag	1
Command Monitors	13
Spares	5
TOTAL	48

FIGURE B: RECOMMENDED DISCRETE DATA BITS

Sampling Format: A Recommended Sampling Format is Shown in Figure C Below.

Word No.	Bit Positions		
	1	2 3 4	5 thru 16
1	P	48 Discrete Bits	IR Channel 1
2	P		IR Channel 2
3	P		IR Channel 3
4	P		IR Channel 4
5	P		IR Channel 5
6	P		IR Channel 6
7	P		IR Channel 7
8	P		IR Channel 8
9	P		IR Channel 9
10	P		IR Channel 10
11	P		IR Channel 11
12	P		IR Channel 12
13	P		IR Channel 13
14	P		IR Channel 14
15	P		Temperature Sub Com 1
16	P		Temperature Sub Com 2

FIGURE C: TOVS SAMPLING FORMAT

DESCRIPTION OF INSTRUMENT COMMANDS

TOVs operating modes are directly controlled by thirteen (13) space craft supplied commands.

Command Subsystem: A command subsystem is required to execute the commands obtained from the TIROS-N S/C command system.

TOVS command subsystem is similar to that used on ITPR in that the same type of hardware implementation is recommended.

Command List: A total of thirteen (13) commands are required to control the TOVS. Each of these commands, together with a description of the action, is shown in Table A.

Command Circuitry Description: Magnetic latching relays are recommended as the storage devices for all radiometer commands. A typical command relay is shown in Figure B.

Although the exact spacecraft interface is not defined in the technical specification; it is assumed that the relays will be driven by one (1) MA type line and one (1) MB type line.

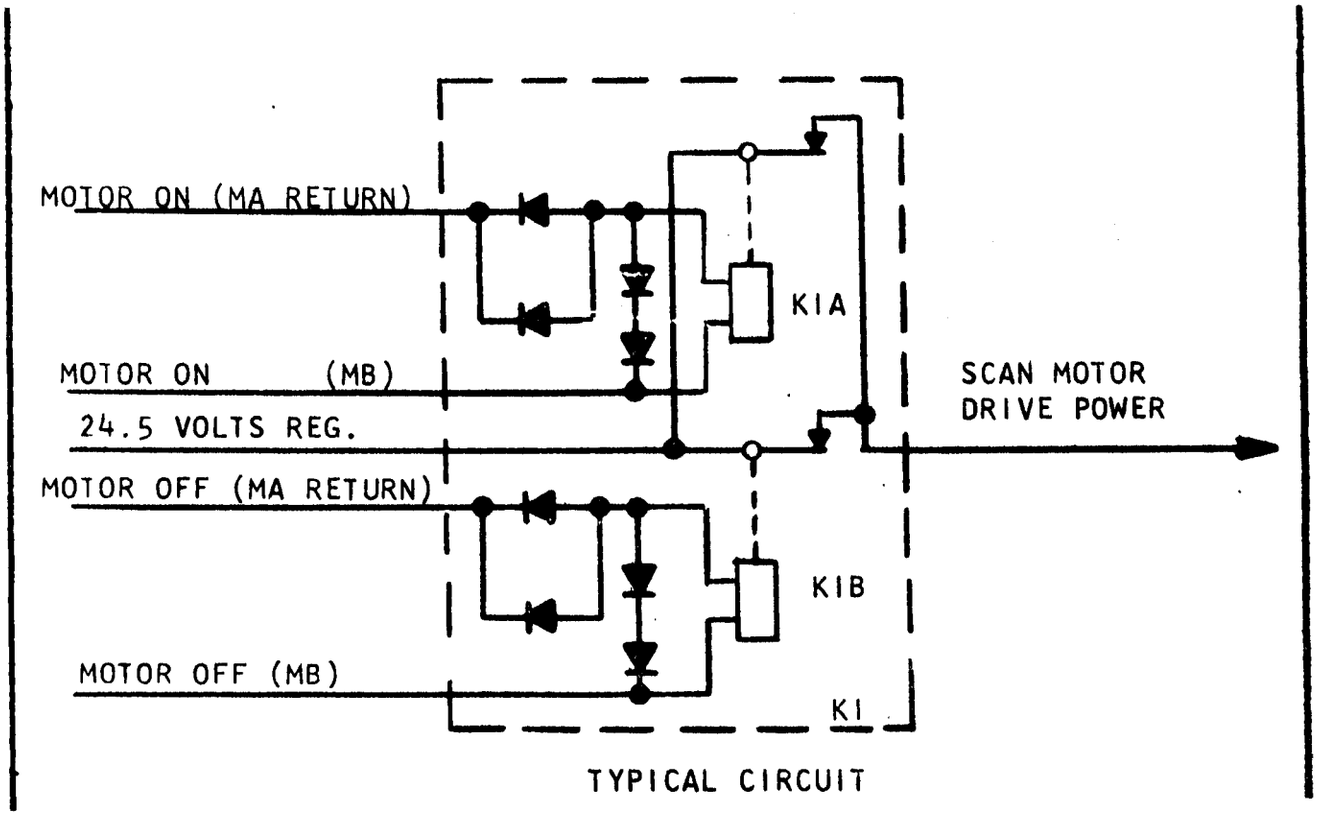


FIGURE B: COMMAND LATCHING RELAY CIRCUIT

TABLE A: TOVS COMMAND LIST

COMMAND	RESPONSE
1. Chopper Motor ON/OFF	Applies/Disconnects power to the chopper motor drive circuit.
2. Electronics ON/OFF	Applied/Disconnects power to all TOVS electronics, causing all channels to become inactive.
3. Scan Drive ON/OFF	Applies/Disconnects power to the scan motor drive circuit.
4. IR Calibrate ON/OFF	Enables/disables the automatic in-flight calibration cycle of space and housing.
5. Electronic Calibration ON/OFF	Enables/disables the electronic calibration of integrator, multiplexer and ADC.
6. NADIR Position ON/OFF	Causes the scan mirror to view the nadir position.
7. Space Position ON/OFF	Causes the scan mirror to view the space position.
8. Housing Position ON/OFF	Causes the scan mirror to view the housing position.
9. Detector Temperature Controller ON/OFF	Applies/disconnects power to the detector temperature controller.
10. Calibration Black Body Heater ON/OFF	Applies/disconnects power to the black body heater.
11. Standby Heater ON/OFF	Applies/disconnects power to the instrument standby heater.
12. Restricted Scan ON/OFF	Causes the scan program to be restricted to 1/2 the normal range.
13. Dual Instrument Mode ON/OFF	Causes TOVS A and B to process data at 1/2 normal rate.